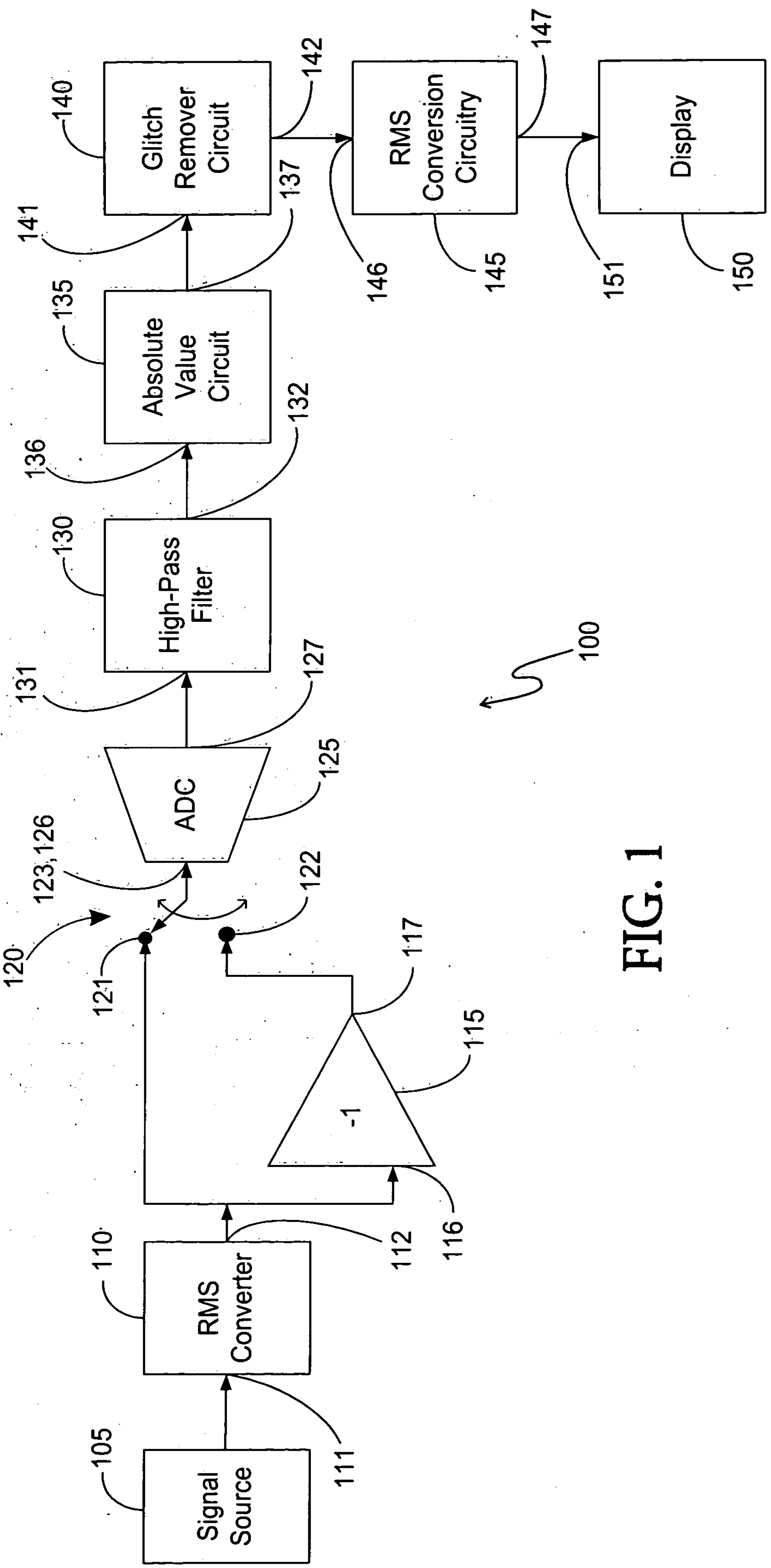
Signal Source
105
111
RMS Converter
110
112
116
-1
115
117
121
120
122
123,126
ADC
125
127
131
High-Pass Filter
130
132
136
Absolute Value Circuit
135
137
141
Glitch Remover Circuit
140
142
146
RMS Conversion Circuitry
145
147
151
Display
150
100

FIG. 1

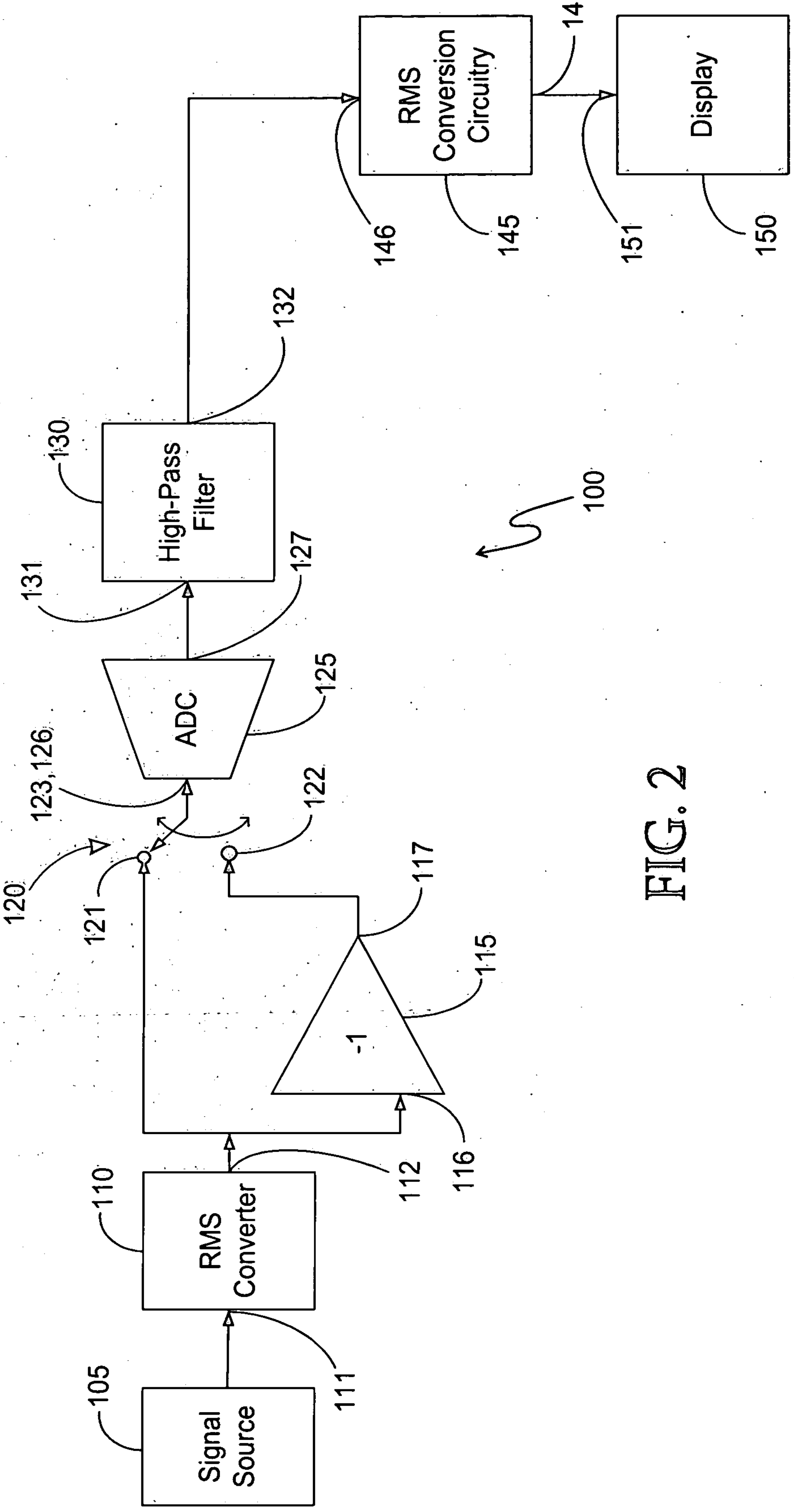
Signal Source
105
111
RMS Converter
110
112
116
-1
115
117
121
122
120
123,126
ADC
125
127
131
High-Pass Filter
130
132
146
RMS Conversion Circuitry
145
147
151
Display
150
100

FIG. 2

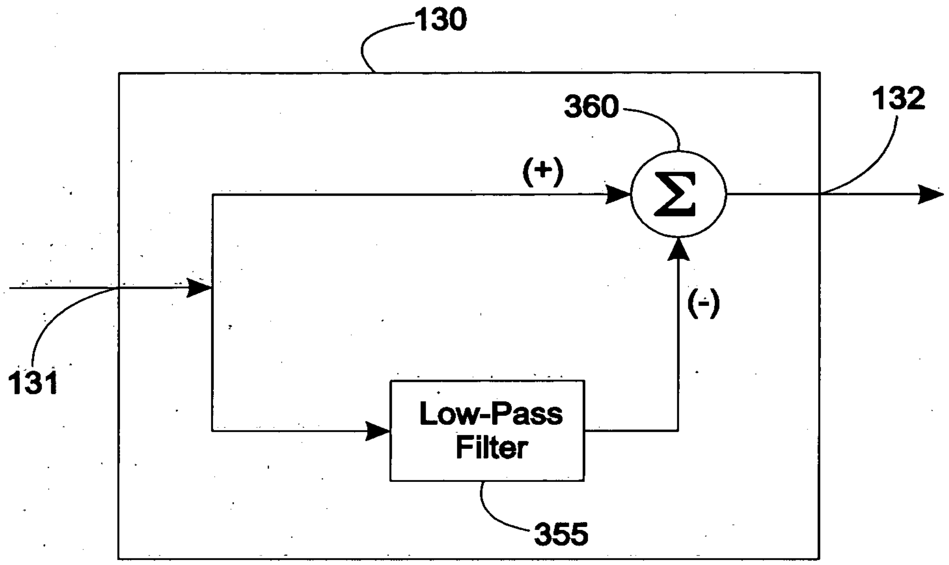
130
360
132
(+)
Σ
(-)
131
Low-Pass Filter
355

FIG. 3

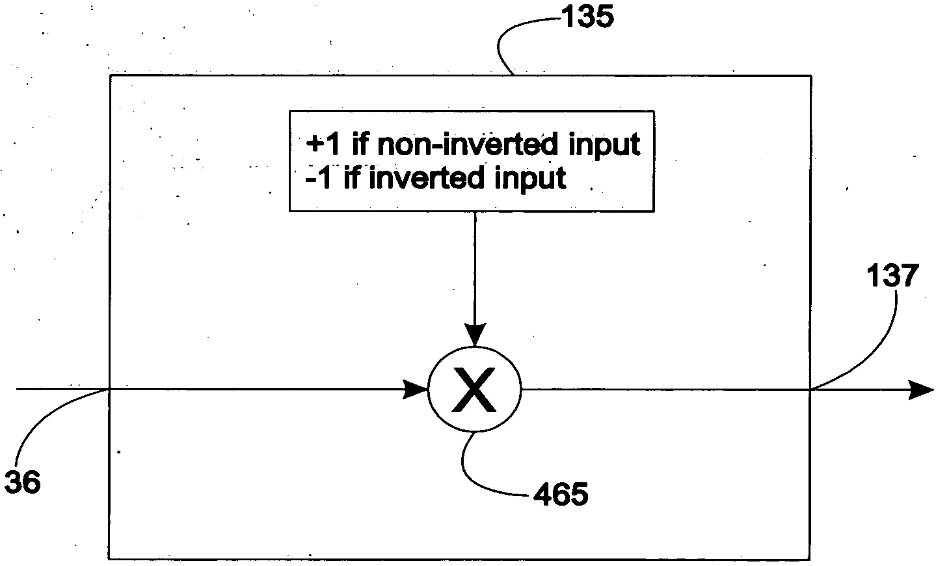
135
+1 if non-inverted input
-1 if inverted input
137
X
136
465

FIG. 4

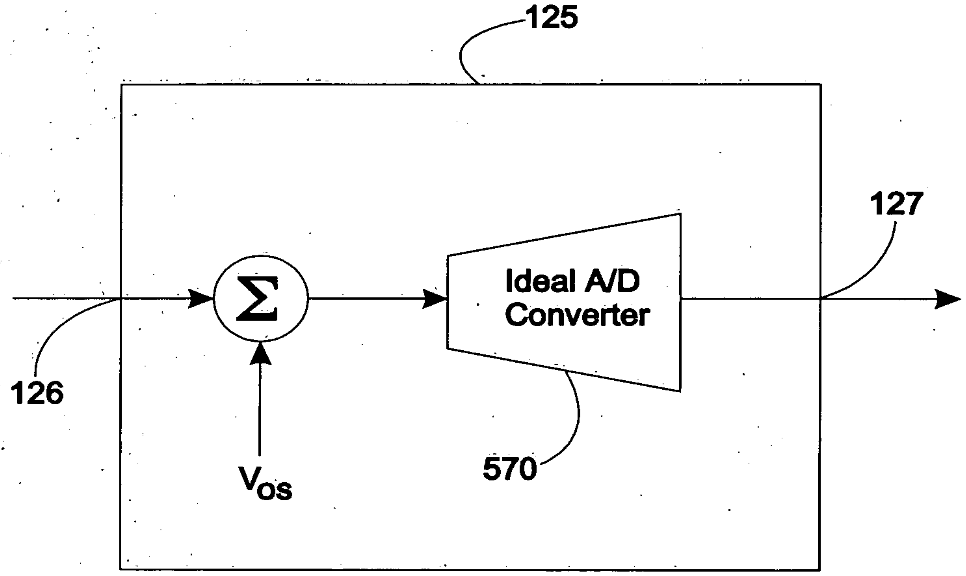

FIG. 5

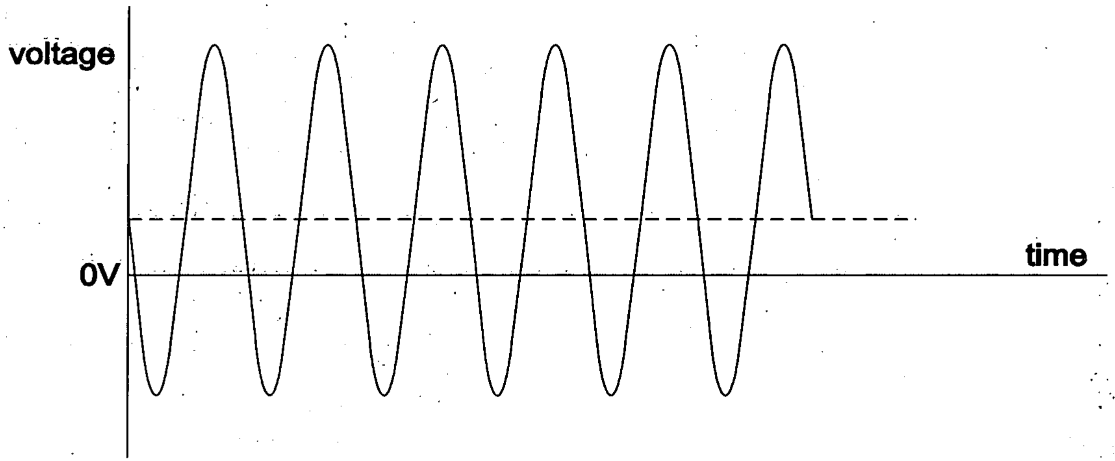

FIG. 6A

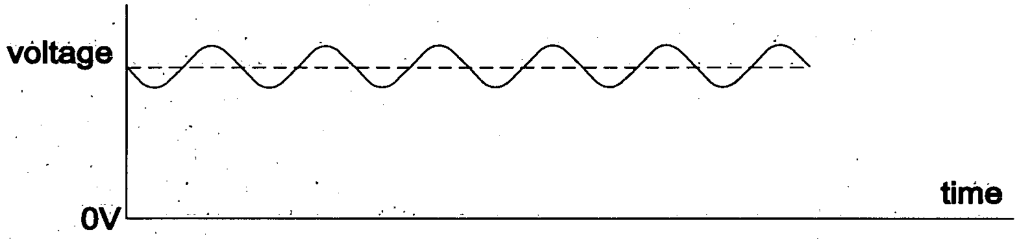

FIG. 6B

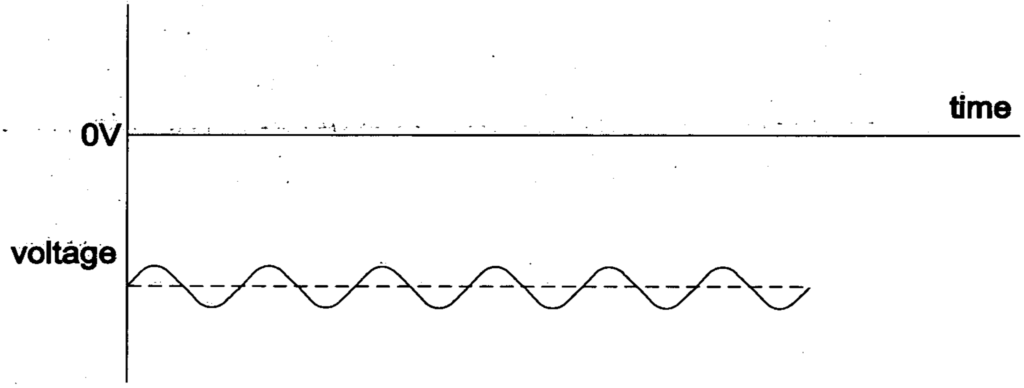

FIG. 6C

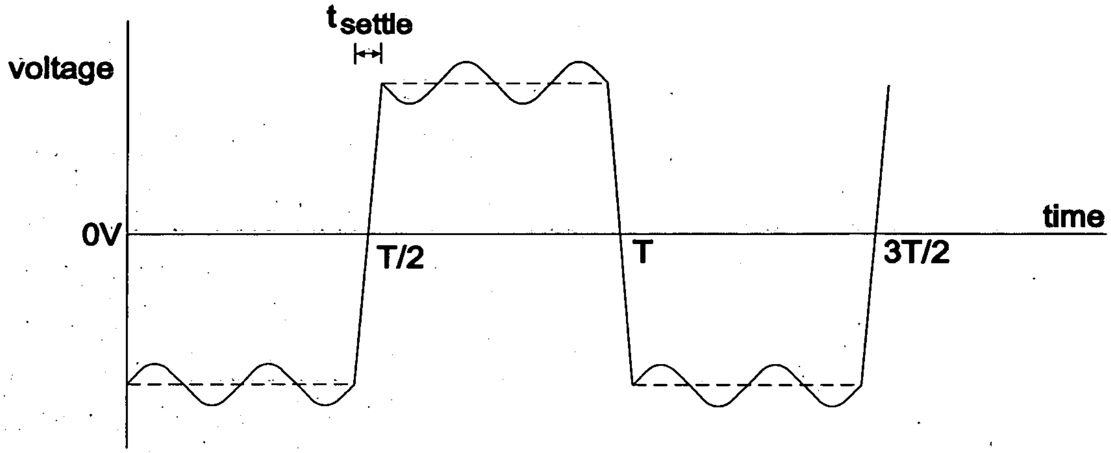
t_{settle}
voltage
0V
time
T/2
T
3T/2

FIG. 6D

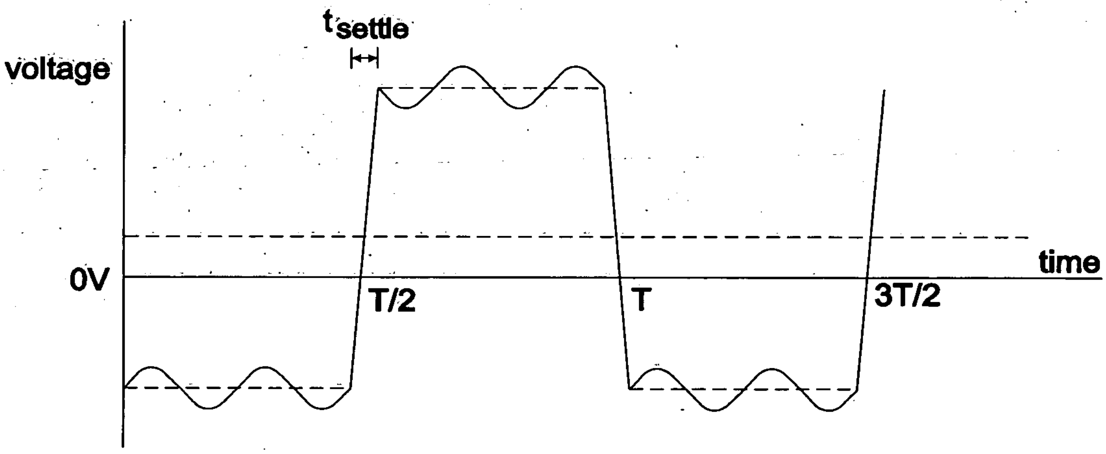
t_{settle}
voltage
0V
time
T/2
T
3T/2

FIG. 6E

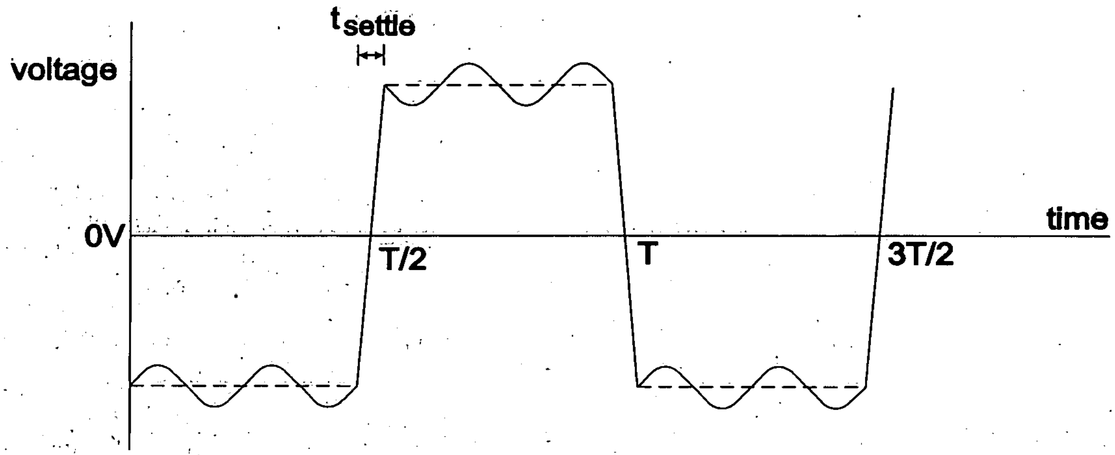
t_{settle}
voltage
0V
time
T/2
T
3T/2

FIG. 6F

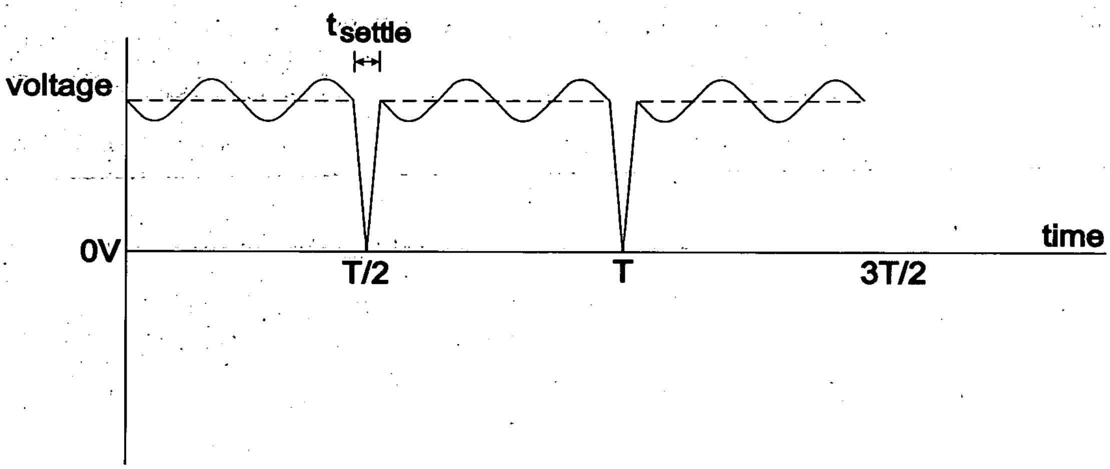
t_{settle}
voltage
0V
time
T/2
T
3T/2

FIG. 6G

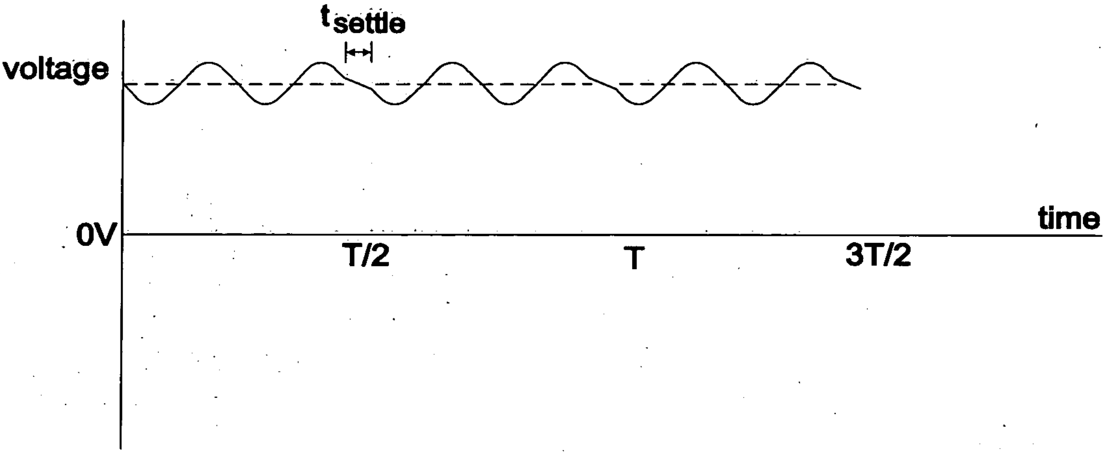

FIG. 6H

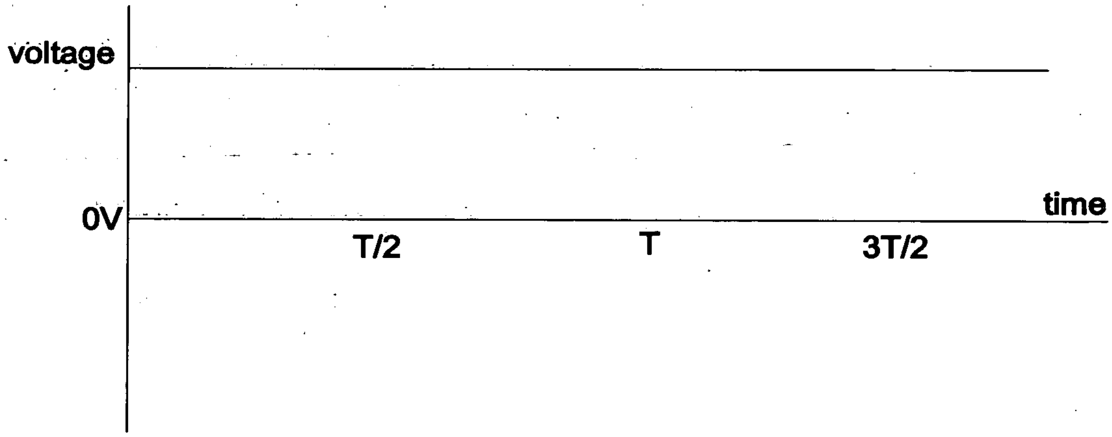

FIG. 6I

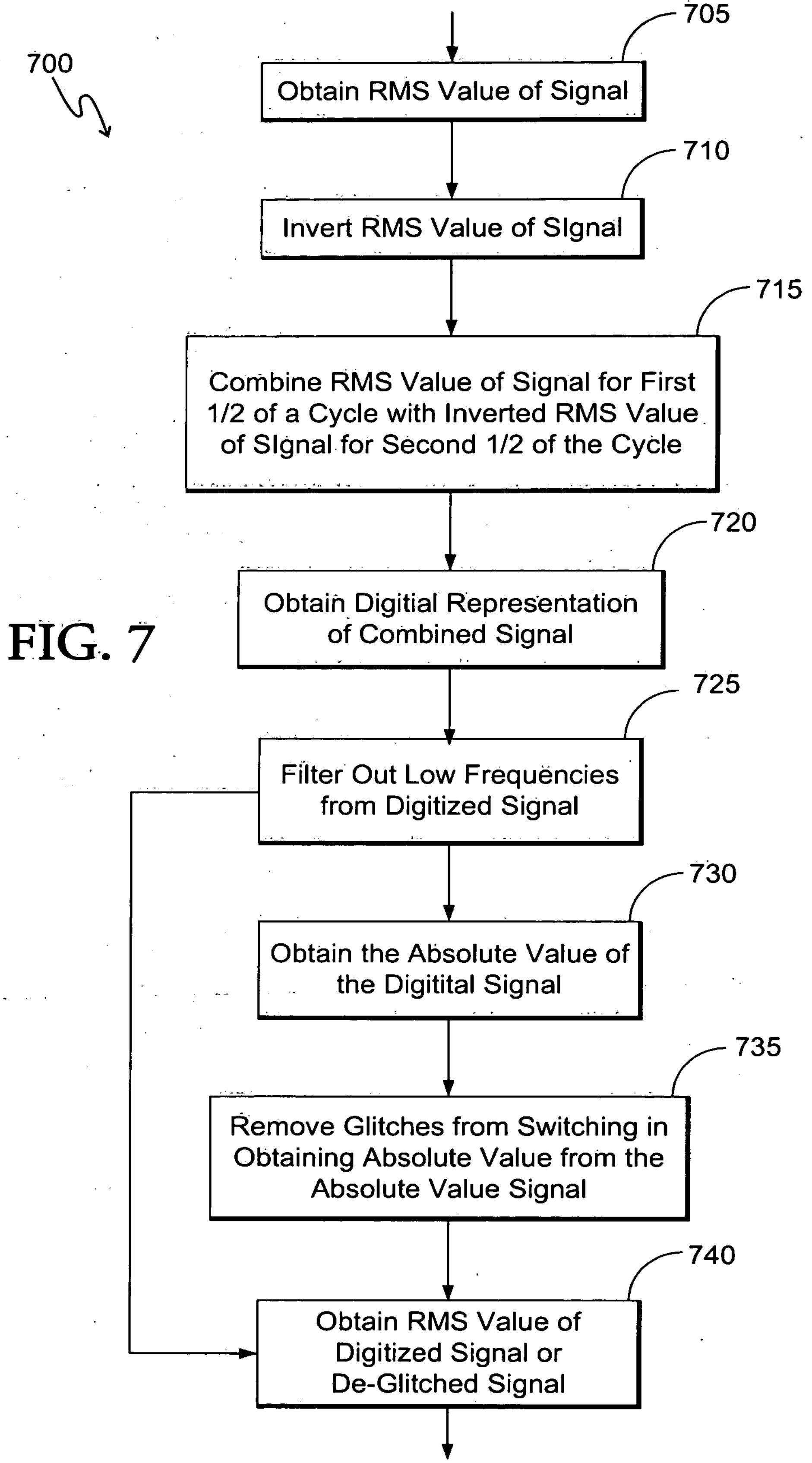
700
705
Obtain RMS Value of Signal
710
Invert RMS Value of SIgnal
715
Combine RMS Value of Signal for First 1/2 of a Cycle with Inverted RMS Value of SIgnal for Second 1/2 of the Cycle
720
Obtain Digitial Representation of Combined Signal
725
Filter Out Low Frequencies from Digitized Signal
730
Obtain the Absolute Value of the Digitital Signal
735
Remove Glitches from Switching in Obtaining Absolute Value from the Absolute Value Signal
740
Obtain RMS Value of Digitized Signal or De-Glitched Signal

FIG. 7